Roll No: 153079029 VLSI DESIGN ASSIGNMENT 1

The method of logical effort allows us to deal with different components of gate delay indepen-dently. Effect of the manufacturing process is represented by τ , which is the delay of a unit inverter driving another unit inverter without including parasitic delay. The effect of loading is represented by h, which is the ratio of load capacitance to input capacitance. The effect of gate topology is represented by g and the delay due to parasitic loading is accounted for by p.

We shall evaluate these parameters for a technology whose model parameters are given at the end of this assignment. We first design a minimum sized inverter with equal rise and fall times at the output.

Q–1 We first design the minimum sized inverter or x1 inverter. Channel length for all transistors will be 0.4µm. Minimum channel width is 0.6µm. Include the drain and source capacitances by specifying ad = as = $2W \times L_{min}$ and pd = ps = $2 \times (W + 2L_{min})$. For this process, we shall take V_{DD} to be 3.3V.

Simulate an inverter taking a minimum sized n channel transistor. Initially take the p channel transistor W/L to be 3 times ($\approx U0_n/U0_p$ in the model file) that of the n channel transistor. Use a load capacitor of 0.1 pF, so that the rise and fall times are large. Adjust the W/L of the p channel transistor till the rise time and fall time of the inverters are equal. This inverter (without the load capacitor) will be our unit inverter (x1). Make a sub-circuit with this inverter. Make sure you give a short enough time step in your .tran statement ($\leq$ 1ps) so that you can evaluate delays of the order of tens of ps accurately.

Ans: **Netlist**

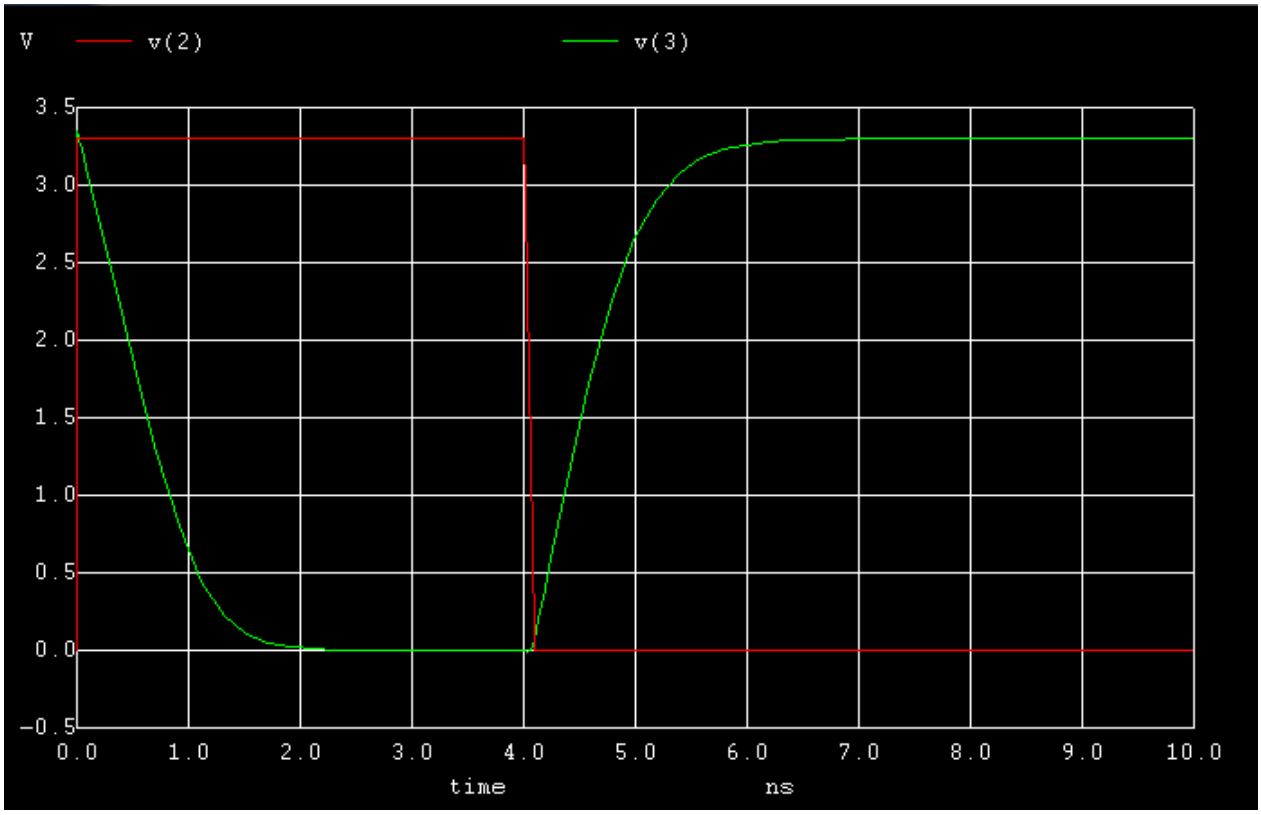
```
inverter
.include model.txt
M1 3 2 0 0 CMOSN L=0.4um W=0.6um ad=0.48p as=0.48p pd=2.8u ps=2.8u
M2 3 2 1 1 CMOSP L=0.4um W=1.5483000um ad=1.23864p as=1.23864p
pd=4.6966u ps=4.6966u
CL 3 0 0.1pF
Vdd 1 0 3.3v
Vin 2 0
Vin 2 0 pwl(0 0v 0.1ps 0v 1ps 3.3v 4ns 3.3v 4.1ns 0)
.tran 8ns 10ns
.MEASURE TRAN risetime TRIG v(3) val=0.33 rise=1 TARG v(3) val=2.97
rise=1
.MEASURE TRAN falltime TRIG v(3) val=2.97 fall=1 TARG v(3) val=0.33
fall=1
.control
run
plot v(3) v(2)
.endc
.end
```

For NMOS, by taking *L=0.4um W=0.6um* and adjusting W/L for PMOS, by taking *L=0.4um W=1.5483000um,* equal rise and fall times are observed.

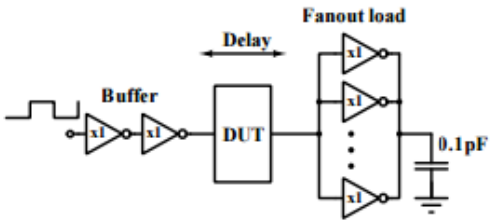
Following is the screenshot of simulation result showing equal rise and fall time of inverter.

```
No. of Data Rows : 90

  Measurements for Transient Analysis

risetime            =  1.088404e-009 targ=  5.257539e-009 trig=  4.169135e-009
falltime            =  1.088402e-009 targ=  1.218580e-009 trig=  1.301780e-010

ngspice 1 ->
```

Graph of Output V/S Input waveform of Inverter.



Q–2 We shall use the following circuit for simulating various gate delays.



We evaluate τ by using a minimum sized inverter as the DUT. Inverters marked as x1 are minimum sized inverters with symmetric rise and fall times. DUT is the gate which is being characterized. The x1 inverters at the input apply a realistic rise time/fall time square wave to the device under test. Such inverter pairs will be used for every input of the DUT. The output will be loaded by different numbers of inverters in parallel.

Inverters forming the fanout load drive a fixed 0.1 pF capacitor. We find the delay while loading it with 1, 2, 3, ...6 inverters and plotting the delay (in absolute units) versus h. For an inverter, $g = 1$ (by definition) and h here is just the fanout.

$$d_{abs} = (gh + p)\tau = h\tau + p_{inv}\tau$$

We expect the delay plot to be a straight line, with a slope of τ and the y intercept of $p_{inv}\tau$. Evaluate τ and p_{inv}.

Ans: **Netlist:**

inverter
.include model.txt
.subckt inverter in out gnd vdd
M1 out in gnd gnd CMOSN L=0.4um W=0.6um ad=0.48p as=0.48p pd=2.8u ps=2.8u
M2 out in vdd vdd CMOSP L=0.4um W=1.5483000um ad=1.23864p as=1.23864p pd=4.6966u ps=4.6966u
.ends inverter
V1 vdd gnd dc 3.3v
X1 in1 out1 gnd vdd inverter
X2 out1 out2 gnd vdd inverter
X3 out2 out3 gnd vdd inverter
X4 out3 out4 gnd vdd inverter
X5 out3 out4 gnd vdd inverter
X6 out3 out4 gnd vdd inverter
X7 out3 out4 gnd vdd inverter
X8 out3 out4 gnd vdd inverter
X9 out3 out4 gnd vdd inverter

cl out4 gnd 0.1P

vin in1 gnd PULSE(0 3.3 0 0.1PS 0.1PS 10NS 20NS)

.tran 20ns 30ns
.control
run
MEAS TRAN tau1 TRIG v(out2) val=1.65 rise=1 TARG v(out3) val=1.65 fall=1
MEAS TRAN tau2 TRIG v(out2) val=1.65 fall=1 TARG v(out3) val=1.65 rise=1
*let tau=(tau1+tau2)*0.5*
print tau

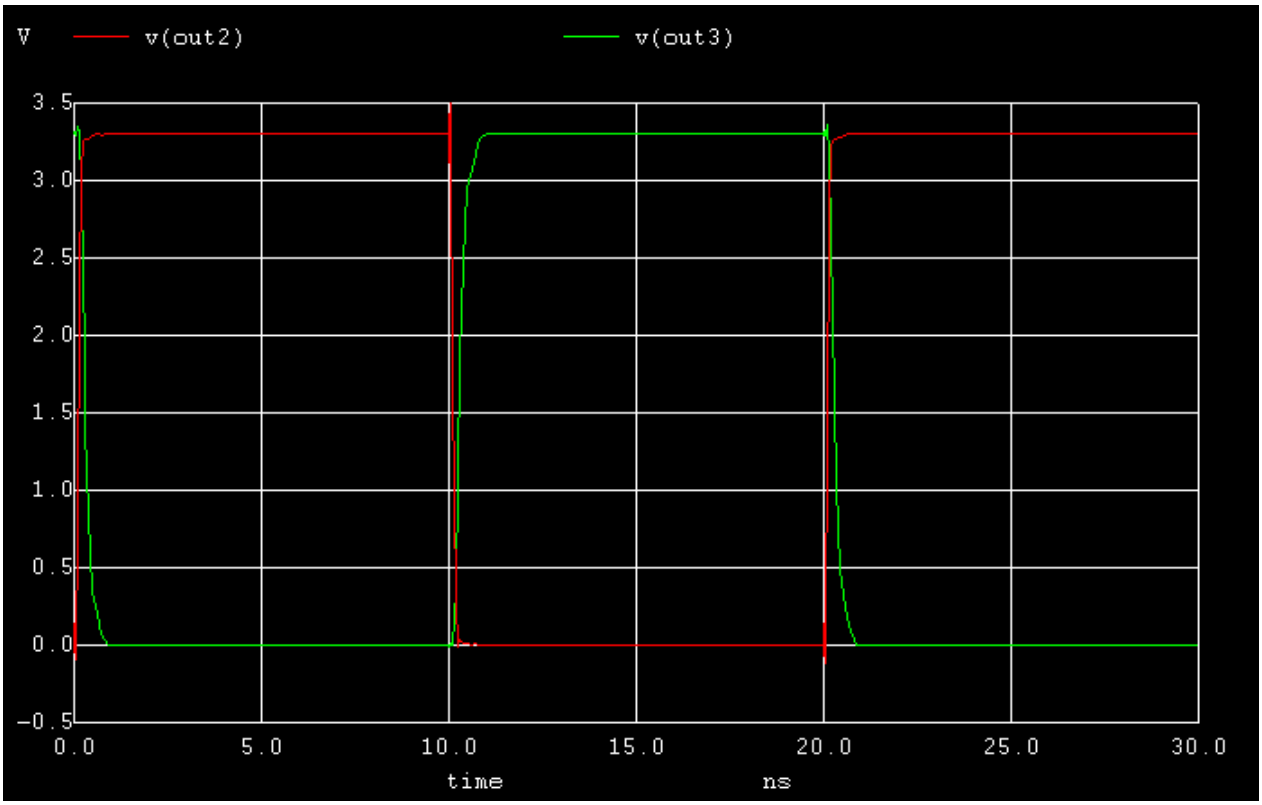
plot v(out3) v(out2)
.endc
.end

Simulation Result :

The simulation result and graph below are shown for only one case out of 6 cases when all six inverters are connected in parallel. The table below shows all the delays considering all 6 cases.

```
Circuit: inverter

Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

Warning: vin: no DC value, transient time 0 value used

Initial Transient Solution
--------------------------

Node                                   Voltage
----                                   -------
vdd                                        3.3
out1                                       3.3
in1                                          0
out2                                1.17246e-008
out3                                       3.3
out4                                1.17246e-008
vin#branch                                   0
v1#branch                          -4.28021e-011



No. of Data Rows : 140
tau1                =  1.735782e-010 targ=  2.886521e-010 trig=  1.150739e-010
tau2                =  1.573078e-010 targ=  1.027521e-008 trig=  1.011791e-008
tau = 1.654430e-010
```

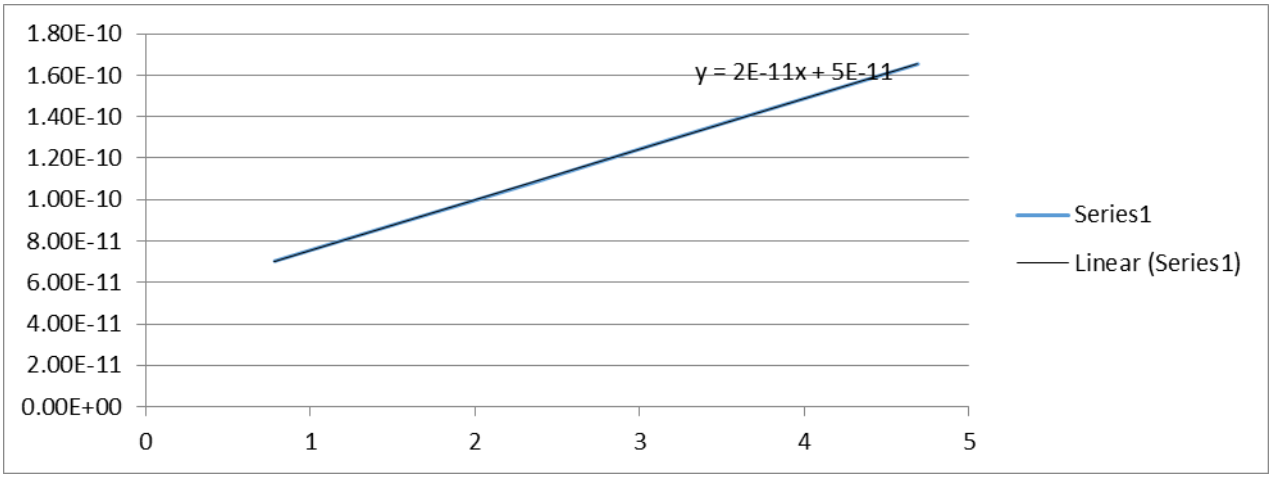
Graph of Output V/S Input of DUT



The following table shows different delay values of inverter for different no. of inverters connected in parallel

	A	B
1	inverter	
2	h	d
3	0.7816	7.03E-11
4	1.5633	8.93E-11
5	2.345	1.08E-10
6	3.1267	1.28E-10
7	3.9084	1.47E-10
8	4.69	1.65E-10
9		

The following is the graphical representation of above tabulated values.



It is seen that the delay plot is a straight line with the slope of 2*10^(-11) which represents τ.
p τ=5*10^(-11).

Q–3 A) Simulate the circuit in the figure above, using a 2 input NAND gate as the DUT. The transistor geometries of the NAND should be scaled from the x1 inverter by the usual series parallel rules. Plot the delay in units of τ versus the fanout and evaluate the logical effort as well as the p value for the NAND gate.

B) Repeat the evaluation of g and p for 2 input NOR gate scaled according to series parallel rules from an x1 inverter.

Ans: **(a) NAND:**

Netlist:

```
Nand
.include model.txt
.subckt inverter in out gnd vdd
M1 out in gnd gnd CMOSN L=0.4um W=0.6um ad=0.48p as=0.48p pd=2.8u
ps=2.8u
M2 out in vdd vdd CMOSP L=0.4um W=1.5483000um ad=1.23864p
as=1.23864p pd=4.6966u ps=4.6966u
.ends inverter

.subckt nand a b d4 gnd vdd
M3 d3 a gnd gnd CMOSN L=0.4um W=1.2um ad=0.96p as=0.96p pd=4u
ps=4u
M4 d4 b d3 d3 CMOSN L=0.4um W=1.2um ad=0.96p as=0.96p pd=4u ps=4u
M5 d4 a vdd vdd CMOSP L=0.4um W=1.5483000um ad=1.23864p
as=1.23864p pd=4.6966u ps=4.6966u
M6 d4 b vdd vdd CMOSP L=0.4um W=1.5483000um ad=1.23864p
as=1.23864p pd=4.6966u ps=4.6966u
.ends nand

V1 vdd gnd dc 3.3v
X1 in1 out1 gnd vdd inverter
X2 out1 out2 gnd vdd inverter
X3 out2 vdd out3 gnd vdd nand
X4 out3 vdd out4 gnd vdd nand
X5 out3 vdd out4 gnd vdd nand
X6 out3 vdd out4 gnd vdd nand
X7 out3 vdd out4 gnd vdd nand
X8 out3 vdd out4 gnd vdd nand
X9 out3 vdd out4 gnd vdd nand


cl out4 gnd 0.1P
vin in1 gnd PULSE(0 3.3 0 0.1PS 0.1PS 10NS 20NS)
.tran 10ns 30ns
```

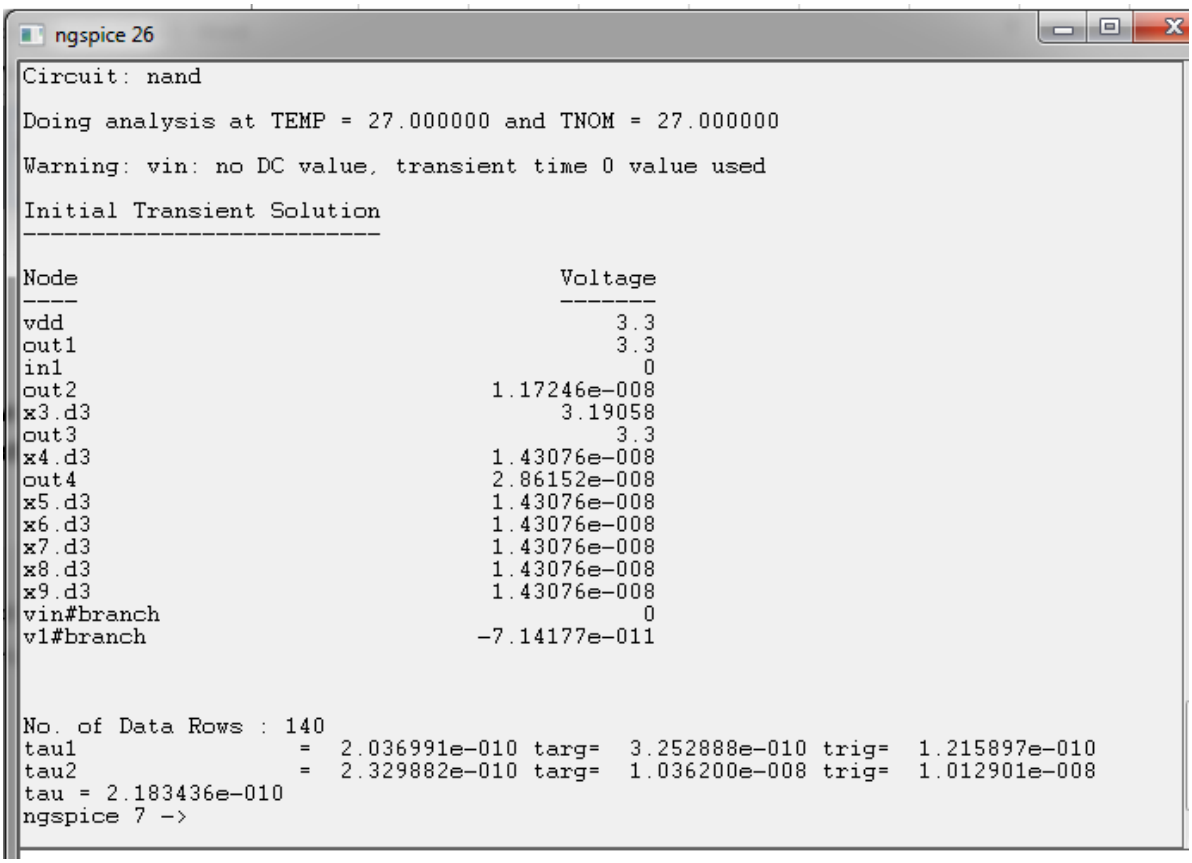
.control
run
MEAS TRAN tau1 TRIG v(out2) val=1.65 rise=1 TARG v(out3) val=1.65 fall=1
MEAS TRAN tau2 TRIG v(out2) val=1.65 fall=1 TARG v(out3) val=1.65 rise=1
*let tau=(tau1+tau2)*0.5*
print tau

plot v(out3) v(out2)
.endc

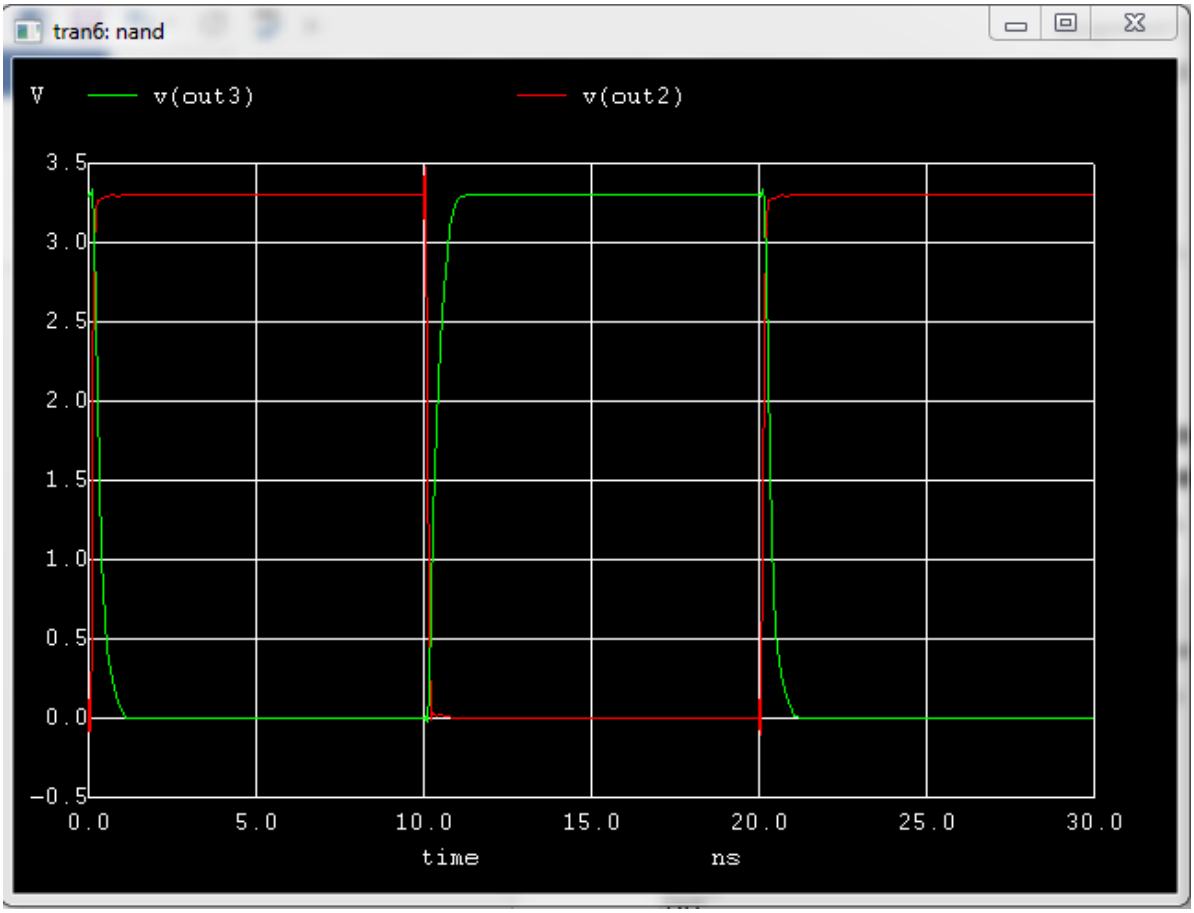
.end

Simulation Result :

The simulation result and graph below are shown for only one case out of 6 cases when all six inverters are connected in parallel. The table below shows all the delays considering all 6 cases.



Graph of Output V/S Input of DUT

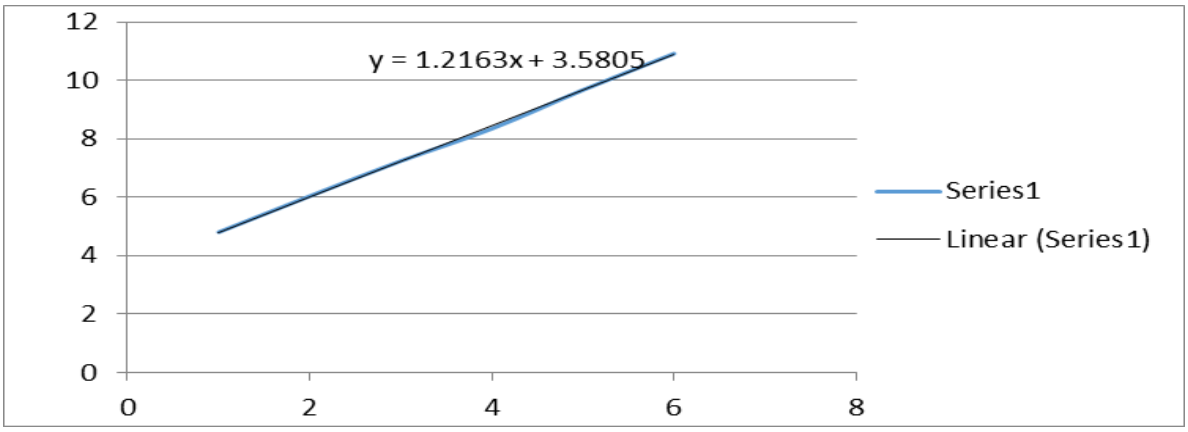


The following table shows different delay values of NAND for different no. of inverters connected in parallel

Note that for NAND and NOR, τ is divided in the delay

49	h	d	c
50	1	4.805054	
51	2	6.03945	
52	3	7.241255	
53	4	8.34919	
54	5	9.67358	
55	6	10.91718	

The following is the graphical representation of above tabulated values.



From the above graph it can be seen that,
Logical Effort = 1.2163
P value of NAND Gate = 3.5805

(b) **NOR:**

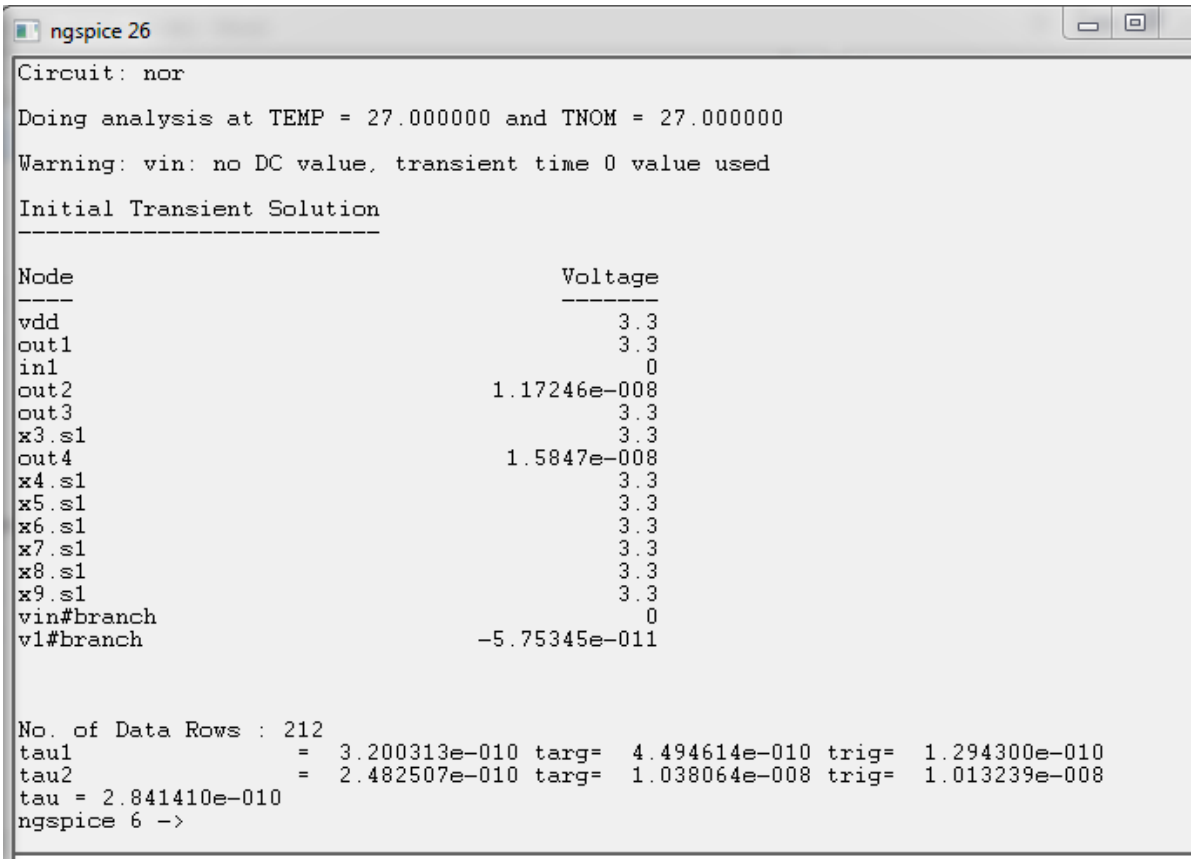
Netlist:

```
NOR
.include model.txt
.subckt inverter in out gnd vdd
M1 out in gnd gnd CMOSN L=0.4um W=0.6um ad=0.48p as=0.48p pd=2.8u
ps=2.8u
M2 out in vdd vdd CMOSP L=0.4um W=1.5483000um ad=1.23864p
as=1.23864p pd=4.6966u ps=4.6966u
.ends inverter

.subckt nor a b d1 gnd vdd
M3 d1 a gnd gnd CMOSN L=0.4um W=0.6um ad=0.48p as=0.48p pd=2.8u
ps=2.8u
M4 d1 b gnd gnd CMOSN L=0.4um W=0.6um ad=0.48p as=0.48p pd=2.8u
ps=2.8u
M5 d1 a s1 s1 CMOSP L=0.4um W=3.0966um ad=4.95456p as=4.95456p
pd=13.9864u ps=13.9864u
M6 s1 b vdd vdd CMOSP L=0.4um W=3.0966um ad=4.95456p as=4.95456p
pd=13.9864u ps=13.9864u

.ends nor

V1 vdd gnd dc 3.3v
X1 in1 out1 gnd vdd inverter
X2 out1 out2 gnd vdd inverter
X3 out2 gnd out3 gnd vdd nor
X4 out3 gnd out4 gnd vdd nor
X5 out3 gnd out4 gnd vdd nor
X6 out3 gnd out4 gnd vdd nor
X7 out3 gnd out4 gnd vdd nor
X8 out3 gnd out4 gnd vdd nor
X9 out3 gnd out4 gnd vdd nor


cl out4 gnd 0.1P
vin in1 gnd PULSE(0 3.3 0 0.1pS 0.1pS 10NS 20NS)
.tran 10ns 50ns
```

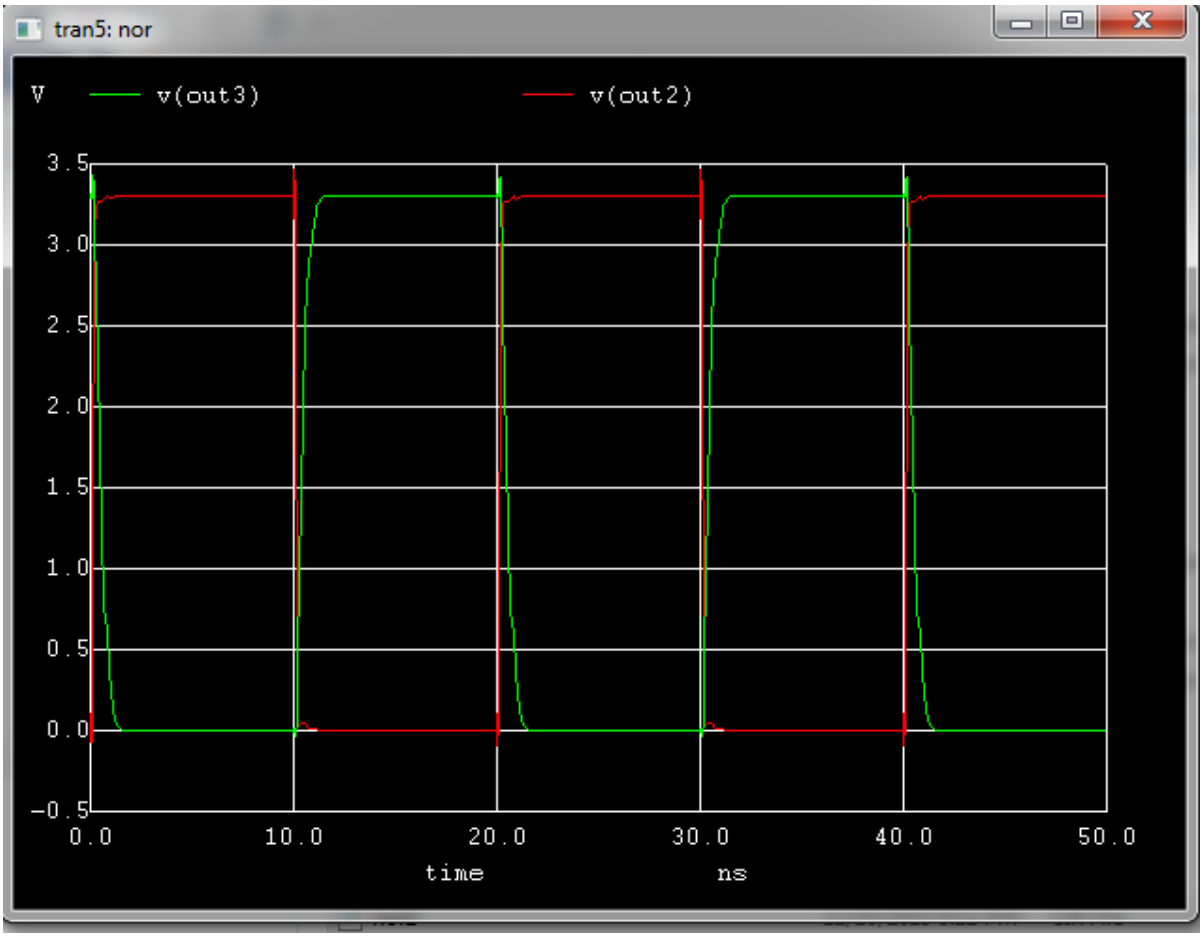
```
.control
run
MEAS TRAN tau1 TRIG v(out2) val=1.65 rise=1 TARG v(out3) val=1.65
fall=1
MEAS TRAN tau2 TRIG v(out2) val=1.65 fall=1 TARG v(out3) val=1.65
rise=1
let tau=(tau1+tau2)*0.5
print tau

plot v(out3) v(out2)
.endc

.end
```

Simulation Result :

The simulation result and graph below are shown for only one case out of 6 cases when all six inverters are connected in parallel. The table below shows all the delays considering all 6 cases.



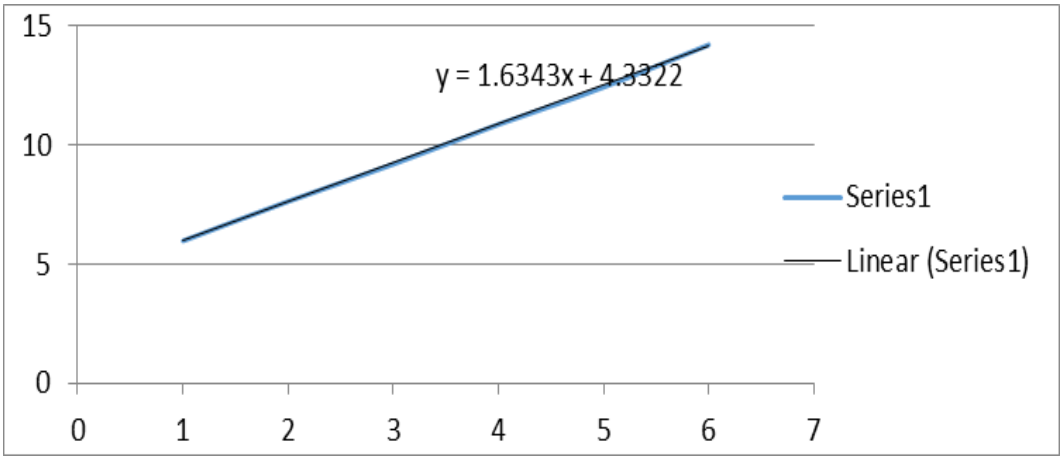
Graph of Output V/S Input of DUT



The following table shows different delay values of NOR for different no. of inverters connected in parallel

	h	d
57	h	d
58	1	5.97607
59	2	7.638205
60	3	9.196855
61	4	10.86422
62	5	12.43089
63	6	14.20705

The following is the graphical representation of above tabulated values.



From the above graph it can be seen that,
Logical Effort = 1.6343
P value of NAND Gate = 4.3322